## REMARKS

Claims 50-66 were rejected. Claims 50, 55, 62, and 66 have been amended. Claims 38-49 were previously withdrawn in response to a restriction requirement mailed September 5, 2008. Accordingly, claims 38-66 are pending. Reconsideration of the pending claims is respectfully requested.

*Claim Rejections – 35 U.S.C. § 103*

Claims 50-66 were rejected under 35 U.S.C. § 103(a) over US Patent No. 5,754,233 to Takashima in view of U.S. Patent No. 5,812,699 to Zhu et al. ("Zhu"). Applicants respectfully traverse the rejections.

In the Response to Arguments section of the Final Office Action, the Examiner argues that Takashima teaches the "counter" and Zhu teaches the "value of the bit counter," and that since "they are both in the compression environment, ..they are combinable to render the claimed invention." However, the Examiner gives no substantive response addressing the arguments presented on at least pages 10-12 of the Response as to why the suggested combination fails to support a finding of obviousness. The Examiner is **completely silent** to the presented arguments that if timing circuit 105 were to process the alleged uncompressed byte count in a manner similar to the pre-processor 105 of Takashima, this would require a **substantial reconstruction** and **redesign** of the elements shown in the primary reference as well as a change in the basic principle under which the construction was designed to operate. Instead on page 5 of the Office Action the Examiner repeats arguments related to the teaching of the disparate elements, which although the Applicants may disagree, did not dispute in the most recently filed Response.

Applicant notes that on pages 7 of the Final Office Action, the Examiner points out that "reasonable inferences which the artisan would have logically drawn therefrom may be properly evaluated in formulating a rejection [under 35 U.S.C. 103(a)]," and that "the obviousness may be made from common knowledge and common sense of a person of ordinary skill in the art without any specific hint or suggestion an a particular

reference." Yet, the Examiner is completely silent as to what sort of "reasonable inference" or "common sense of a person of ordinary skill in the art" would lead the person of ordinary skill in the art to make the suggested modification, especially in light of the Applicants arguments that there is no suggestion when a substantial reconstruction and redesign of the elements is required.

Applicants respectfully submit that because the Office has failed to show how one of ordinary skill could have combined the elements in Zhu and Takashima, without substantial reconstruction and redesign of the elements, a conclusion of obviousness cannot be supported.

Applicants note that claim 55 is patentable over Takashima and Zhu for at least an additional independent reason. For example, claim 55 has been amended to include the previous recitations of now-canceled dependent claim 66.

Amended claim 55 now recites, in pertinent part:

"a controller coupled to said processor to determine a capability of a codec under the control of the processor to compress image data based on whether a difference between a compression time for a current frame and a target frame period exceeds a threshold, *wherein the compression time is based at least in part upon a quantization parameter determined by the processor to fall within an upper and a lower limit for each row of macroblocks in the current frame* (emphasis ours)."

In item 2 of the Office Action, the Examiner has cited timing control unit 105 illustrated in Takashima as corresponding to the claimed processor. The Examiner also has cited counter 104, rate control circuit 107, and buffer counter 108 as together corresponding to the claimed controller. However, in rejecting claim 66, the Examiner has cited rate control circuit 107 as corresponding to the claimed processor that calculates and selects a "quantization parameter" to "fall within an upper and a lower limit for each row of macroblocks in the current frame." Applicants note that the quantization circuit 106c of Takashima "quantizes the DCT coefficients from the DCT circuit 106b at an arbitrary quantization step Q, under the control of the rate control circuit 107,"(col. 8 lines 15-17, Takashima). However, Applicants have been unable to find any teaching in Takashima that rate control circuit 107 "determine[s]"…"a quantization parameter…to fall within an *upper and a lower limit* for *each row of macroblocks in the current frame*."

Furthermore, the rate control circuit 107 is **a wholly different element** than the timing control unit 105 which the Examiner has characterized as the claimed processor. The rate control circuit 107 of Takashima does not receive, "separate from uncompressed image data stored in a first data storage queue, a respective current byte count of a current frame of the uncompressed image data stored in the first data storage queue and receiving separate from compressed image data stored in a second data storage queue, a current byte count of the compressed image data stored in the second data storage queue, to … facilitate an adjusting of a target frame rate," as is required by the processor of claim 1. Applicants note that nor does the timing control unit 105 "determine(s)" a "quantization parameter" to "fall within an upper and a lower limit for each row of macroblocks in the current frame." The characterized elements of Takashima simply do not map to the claim elements.

Accordingly, Applicants respectfully submit that claims 50 and 62 include one or more similar unobvious elements and are patentable over Takashima in view of Zhu. As for dependent claims 51 – 54, 56 – 61, and 63-66, these claims depend from independent claims 50, 55, or 62 incorporating their recitations. Thus, for at least the reason that claims 50, 55, or 62 are patentable over Takashima as described above, claims 51 – 54, 56 – 61, and 63-66 are likewise patentable over Takashima.

Thus, for at least the foregoing reasons, Applicants request that the instant §103 rejections of claims 50 – 66 be withdrawn.

## CONCLUSION

In view of the foregoing remarks, Applicants believe the applicable rejections have been overcome and all claims remaining in the application are presently in condition for allowance. Accordingly, favorable consideration and a Notice of Allowance are earnestly solicited. The Examiner is invited to telephone the undersigned representative at (206) 407-1561 if the Examiner believes that an interview might be useful for any reason.

It is not believed that extensions of time are required beyond those that may otherwise be provided for in documents accompanying this paper. However, if

additional extensions of time are necessary to prevent abandonment of this application, then such extensions of time are hereby petitioned under 37 C.F.R. § 1.136(a).

If any fees are due in connection with filing this paper, the Commissioner is authorized to charge the Deposit Account of Schwabe, Williamson and Wyatt, P.C., No. 50-0393.

Respectfully submitted,
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